

WHAT IS CLAIMED IS:

1. A method for digitizing a signal, comprising:  
sampling and holding an analog signal to yield a  
sampled signal, the analog signal comprising information;  
5 filtering the sampled signal at a passive filter  
circuit to yield a filtered signal, the passive filter  
circuit comprising at least one passive element, the  
filtered signal characterized by a bandpass response; and  
quantizing the filtered signal to yield a digital  
10 signal, the digital signal corresponding to the analog  
signal, the digital signal comprising the information.

2. The method of Claim 1, wherein the analog  
signal comprises an intermediate frequency signal.

3. The method of Claim 1, wherein the passive  
filter circuit comprises a passive bandpass loop filter.

4. The method of Claim 1, wherein the passive  
20 filter circuit comprises at least one filter path, each  
filter path comprising a highpass filter.

5. The method of Claim 1, wherein:

the passive filter circuit further comprises a  
switched capacitor circuit; and

5 filtering the sampled signal at the passive filter  
circuit to yield the filtered signal further comprises:

receiving at least one timing signal and at  
least one control signal;

10 switching the switched capacitor circuit using  
the at least one timing signal to yield a highpass  
filtered signal, the highpass filtered signal  
characterized by a highpass response; and

15 interleaving the highpass filtered signal with  
the at least one control signal to yield the filtered  
signal, the filtered signal characterized by the bandpass  
response.

6. The method of Claim 1, further comprising  
mixing at least two voltage inputs to yield the analog  
signal in a current mode.

7. A sigma-delta modulator, comprising:

a sample-hold circuit operable to sample and hold an analog signal to yield a sampled signal, the analog signal comprising information;

5 a passive filter circuit coupled to the sample-hold circuit and operable to filter the sampled signal to yield a filtered signal, the passive filter circuit comprising at least one passive element, the filtered signal characterized by a bandpass response; and

10 a comparator coupled to the passive filter circuit and operable to quantize the filtered signal to yield a digital signal, the digital signal corresponding to the analog signal, the digital signal comprising the information.

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8. The modulator of Claim 7, wherein the analog signal comprises an intermediate frequency signal.

9. The modulator of Claim 7, wherein the passive  
20 filter circuit comprises a passive bandpass loop filter.

10. The modulator of Claim 7, wherein the passive filter circuit comprises at least one filter path, each filter path comprising a highpass filter.

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11. The modulator of Claim 7, wherein the passive filter circuit comprises a switched capacitor circuit, the passive filter circuit further operable to:

5 receive at least one timing signal and at least one control signal;

switch the switched capacitor circuit using the at least one timing signal to yield a highpass filtered signal, the highpass filtered signal characterized by a highpass response; and

10 interleave the highpass filtered signal with the at least one control signal to yield the filtered signal, the filtered signal characterized by the bandpass response.

15 12. The modulator of Claim 7, further comprising a mixer stage coupled to the passive filter circuit and operable to mix at least two voltage inputs to yield the analog signal in current mode.

13. A sigma-delta modulator, comprising:

a sample-hold circuit operable to sample and hold a next analog signal to yield a sampled signal, the analog signal comprising information;

5 a filter circuit coupled to the sample-hold circuit and operable to filter the sampled signal to yield a filtered signal, the passive filter circuit comprising at least one passive element, the filtered signal characterized by a bandpass response;

10 a comparator coupled to the passive filter circuit and operable to quantize the filtered signal to yield a digital signal, the digital signal corresponding to the analog signal, the digital signal comprising the information; and

15 a feedback loop coupled to the comparator and to the sample-hold circuit and operable to transmit a feedback signal from the comparator to the sample-hold circuit.

20 14. The modulator of Claim 13, wherein the analog signal comprises an intermediate frequency signal.

15. The modulator of Claim 13, wherein the filter circuit comprises a passive bandpass loop filter.

25 16. The modulator of Claim 13, wherein the filter circuit comprises at least one filter path, each filter path comprising a highpass filter.

17. The modulator of Claim 13, the filter circuit further comprising a switched capacitor circuit, the filter circuit further operable to:

5 receive at least one timing signal and at least one control signal;

switch the switched capacitor circuit using the at least one timing signal to yield a highpass filtered signal, the highpass filtered signal characterized by a highpass response; and

10 interleave the highpass filtered signal with the at least one control signal to yield the filtered signal, the filtered signal characterized by a bandpass response.

15 18. The modulator of Claim 13, further comprising a mixer stage coupled to the filter circuit and operable to mix at least two voltage inputs to yield the next analog signal in current mode.

19. A sigma-delta modulator, comprising:

means for sampling and holding an analog signal to yield a sampled signal, the analog signal comprising information;

5 means for filtering the sampled signal to yield a filtered signal, the passive filter circuit comprising at least one passive element, the filtered signal characterized by a bandpass response; and

10 means for quantizing the filtered signal to yield a digital signal, the digital signal corresponding to the analog signal, the digital signal comprising the information.

20. A sigma-delta modulator, comprising:

5 a sample-hold circuit operable to sample and hold a next analog signal to yield a sampled signal, the analog signal comprising information, the analog signal comprising an intermediate frequency signal;

10 a filter circuit coupled to the sample-hold circuit and operable to filter the sampled signal to yield a filtered signal, the passive filter circuit comprising at least one passive element, the filtered signal characterized by a bandpass response, the filter circuit comprising a at least one filter path, each filter path comprising a highpass filter, the filter circuit further comprising at least two paths, each path comprising a switched capacitor circuit, the filter circuit further  
15 operable to:

receive at least one timing signal and at least one control signal;

20 switch the switched capacitor circuit using the at least one timing signal to yield a highpass filtered signal, the highpass filtered signal characterized by a highpass response; and

25 interleave the highpass filtered signal with the at least one control signal to yield the filtered signal, the filtered signal characterized by a bandpass response;

30 a comparator coupled to the passive filter circuit and operable to quantize the filtered signal to yield a digital signal, the digital signal corresponding to the analog signal, the digital signal comprising the information;

a feedback loop coupled to the comparator and to the sample-hold circuit and operable to transmit a feedback

signal from the comparator to the sample-hold circuit;  
and

5        a mixer stage coupled to the filter circuit and  
operable to mix at least two voltage inputs to yield the  
next analog signal in current mode.